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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,416	02/27/2002	Tsuyoshi Fujiwara	XA-9630	7388

7590 08/20/2003

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EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,416	FUJIWARA ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,10-12 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,10-12 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-2, 4-6, 10-12, 14-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-6, 10-12, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai (U.S. Patent No. 5,763,306) In view of Basceri et al. (U.S. Patent No. 6,589,839).

Referring to figures 2a-11b, Tsai teaches a manufacturing method of a semiconductor integrated circuit device comprising a memory cell formed of a MISFET and a capacitor formed on a main surface of a semiconductor substrate comprising the steps of:

Forming the MISFET (see figure 2a) on the main surface of the semiconductor substrate (1),

Forming a first insulating film (12) over the MISFET by the plasma CVD method at a temperature of 500-800°C (see col. 5, lines 1-20),

Forming a second insulating film (13) over the first insulating film by the plasma CVD method at a temperature of 500-850°C (see col. 5, lines 1-20),

Forming a trench (17) by etching the insulating film, and

Depositing a silicon film (19) on the insulating film and in the trench, and removing the silicon film on the insulating film to form a lower electrode of the capacitor on the inner wall of the trench,

Forming a rugged surface silicon (20) on the silicon film (19) on the inner surface of the trench (17) to form a lower electrode of the capacitor (30) on the inner wall of the trench (17).

Depositing a capacitor dielectric layer (21) over the silicon layer,

Depositing a second conductive layer constituting an upper electrode of the capacitor (22) on the capacitor dielectric layer.

It is noted that if the temperature of the first insulating layer is 500°C, the second insulating layer 550°C, which higher than the first insulating layer.

However, the reference does not teach removing the silicon film on the second insulating film to leave the silicon film only on an inner surface of the trench, and forming a logic area, and depositing a insulating layer by using high density plasma CVD.

Referring to figures 1-5, Basceri et al. teaches a method of a semiconductor integrated circuit device comprising a memory cell formed of a MISFET and a capacitor formed on a main surface of a semiconductor substrate, removing the silicon film (26) on the second insulating film (22) to leave the silicon film (26) only inner surface of the trench (24).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to removing the silicon film on the second insulating film to

leave the silicon film only on an inner surface of the trench in process Tsai et al. as taught by Basceri et al. because the process would provide a planar surface and also to increase the surface area of the trench.

It is known in the semiconductor art that DRAM structure has a logic area. It is also known in the semiconductor art that to deposit an insulating layer by using high density plasma CVD.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form DRAM structure has a logic area, and to deposit an insulating layer by using high density plasma CVD in process of Tsai because the logic area would control the memory area, and depositing an insulating layer by using high density plasma CVD in process would provide uniformity of the film.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (703) 308-9439, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 7:00AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (703) 308-4940. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN